

T1E1 Layout Guideline

This application note shows the layout considerations, trace widths calculations, and different scenario, for designing products using Dallas Semiconductor/Maxim's T1/E1 products.

Overview

This application note provides guidelines for circuit board layouts of network interfaces using Dallas Semiconductor multi-port T1/E1 transceivers. The guideline uses the DS26528 part as an example, with different scenarios and conditions but is applicable to other Dallas Semiconductor T1/E1 products. The DS26528 is a single-chip 8-port combination framer and line interface unit (LIU) for T1, E1, and J1 applications. Each port is independently configurable, supporting both long-haul and short-haul lines.

Each layout shows the routing between the DS26528, the transformer and the connector. In particular, each layout shows the recommended trace widths to ensure the proper impedance for a given network interface. All layout board stack-ups are the same.

Layout board stackup:

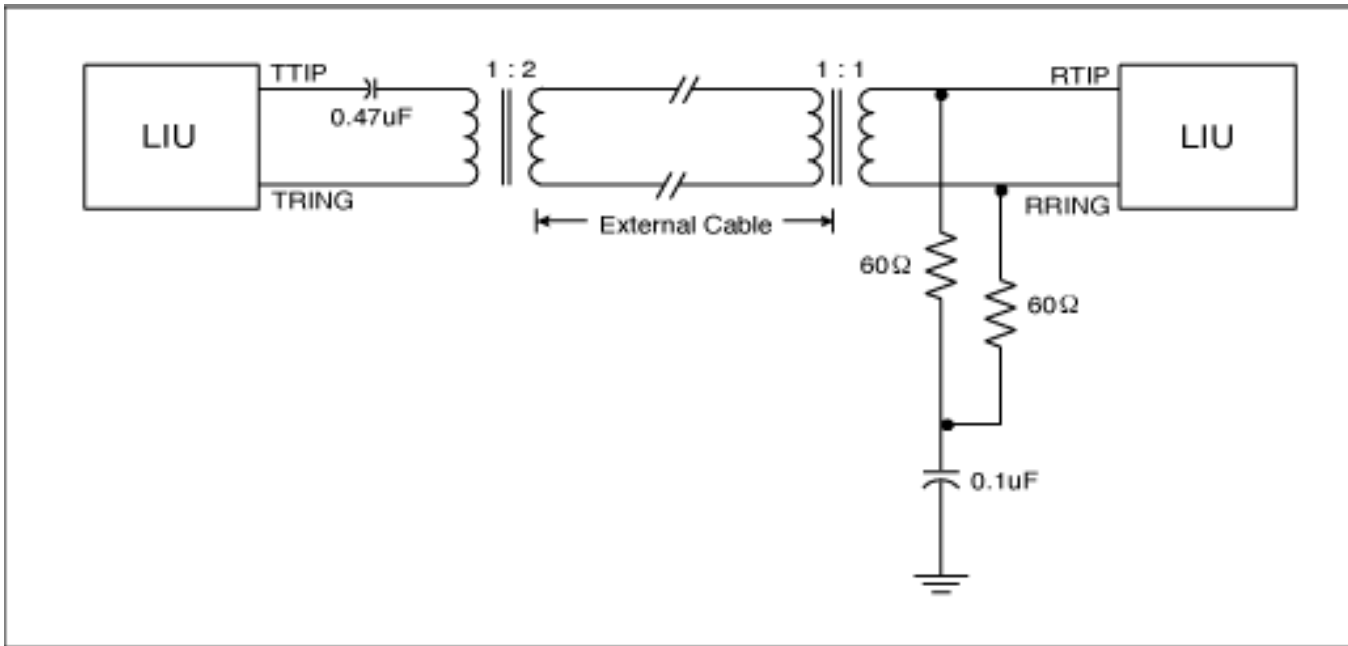
| BOARD STACKUP | |
|------------------|-----------|
| TOP - COPPER | 1.2 MIL |
| DIELECTRIC - FR4 | 5.0 MIL |
| L2_GND - COPPER | 1.2 MIL |
| DIELECTRIC - FR4 | > 5.0 MIL |
| L2_VCC - COPPER | 1.2 MIL |
| DIELECTRIC - FR4 | 5.0 MIL |
| BOT - COPPER | 1.2 MIL |

Layout Considerations:

1. Impedance
2. Location -- keep the signal on the same layer
3. Route TTIP & TRING and RTIP & RRING in parallel to each other
4. Trace widths -- keep traces as short as possible from the DS26528 to the transformer, and

from the transformer to the connector

Basic Network Interface:



Below is an example of the trace width calculation for a T1 interface with 100Ω impedance:

| Surface Materials | Thickness | Dielectric Constant | Line Widths | Impedance |
|-----------------------------|-----------|---------------------|-------------|-----------|
| TTIP and TRING @ 25Ω | | | | |
| Top Conductor Cooper | 1.2MIL | N/A | 25 MIL | 25Ω |
| Dielectric FR-4 | 5MIL | 4.5 | N/A | N/A |
| L2_GND Conductor Copper | 1.2MIL | N/A | N/A | N/A |
| RTIP and RRING @ 50Ω | | | | |
| Top Conductor Cooper | 1.2MIL | N/A | 8.5 MIL | 50Ω |
| Dielectric FR-4 | 5MIL | 4.5 | N/A | N/A |
| L2_GND Conductor Copper | 1.2MIL | N/A | N/A | N/A |

Below is an example of the trace width calculation for an E1 interface with 75Ω impedance:

| Surface Materials | Thickness | Dielectric Constant | Line Widths | Impedance |
|--------------------------------|-----------|---------------------|-------------|-----------|
| TTIP and TRING @ 18.75Ω | | | | |
| Top Conductor Cooper | 1.2MIL | N/A | 35 MIL | 18.75Ω |
| Dielectric FR-4 | 5MIL | 4.5 | N/A | N/A |
| L2_GND Conductor Copper | 1.2MIL | N/A | N/A | N/A |
| RTIP and RRING @ 37.5Ω | | | | |

| | | | | |
|-------------------------|--------|-----|--------|-------|
| Top Conductor Cooper | 1.2MIL | N/A | 14 MIL | 37.5Ω |
| Dielectric FR-4 | 5MIL | 4.5 | N/A | N/A |
| L2_GND Conductor Copper | 1.2MIL | N/A | N/A | N/A |

Below is an example of the trace width calculation for an E1 interface with 120Ω impedance:

| Surface Materials | Thickness | Dielectric Constant | Line Widths | Impedance |
|-----------------------------|-----------|---------------------|-------------|-----------|
| TTIP and TRING @ 30Ω | | | | |
| Top Conductor Cooper | 1.2MIL | N/A | 20 MIL | 30Ω |
| Dielectric FR-4 | 5MIL | 4.5 | N/A | N/A |
| L2_GND Conductor Copper | 1.2MIL | N/A | N/A | N/A |
| RTIP and RRING @ 60Ω | | | | |
| Top Conductor Cooper | 1.2MIL | N/A | 6 MIL | 60Ω |
| Dielectric FR-4 | 5MIL | 4.5 | N/A | N/A |
| L2_GND Conductor Copper | 1.2MIL | N/A | N/A | N/A |

Note: The impedance was calculated with Cadence® Allegro.

Layout Examples

1. The layout of a single E1 port interfacing to BNC connector with 75Ω impedance. All figures are twice the actual size.

Table 1. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|--------|-----|---|----------------------|----------------|
| C1 | 1 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2 | 1 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1, J2 | 2 | Connector BNC 75Ω RA 5 Pin | Trompetor | UCBJR220 |
| R1, R2 | 2 | Resistor 1206 60.4Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| R3, R4 | 2 | Resistor 1206 0Ω 1/8W 5% | Panasonic | ERJ-8GEYJ0R00V |
| T1 | 1 | Transformer, 1CT to 1CT & 1CT to 2CT, 16P SMT | Pulse | T1094 |
| U1 | 1 | Octal Transceiver 0-70C 256P BGA | Dallas Semiconductor | DS26528 |

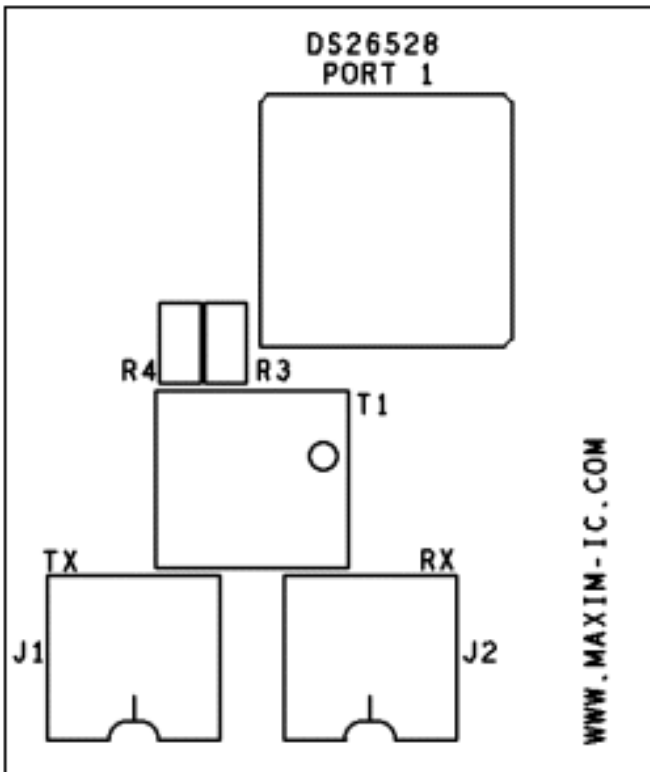


Figure 1.1 E1x1 75Ω impedance -- Silkscreen top layer layout

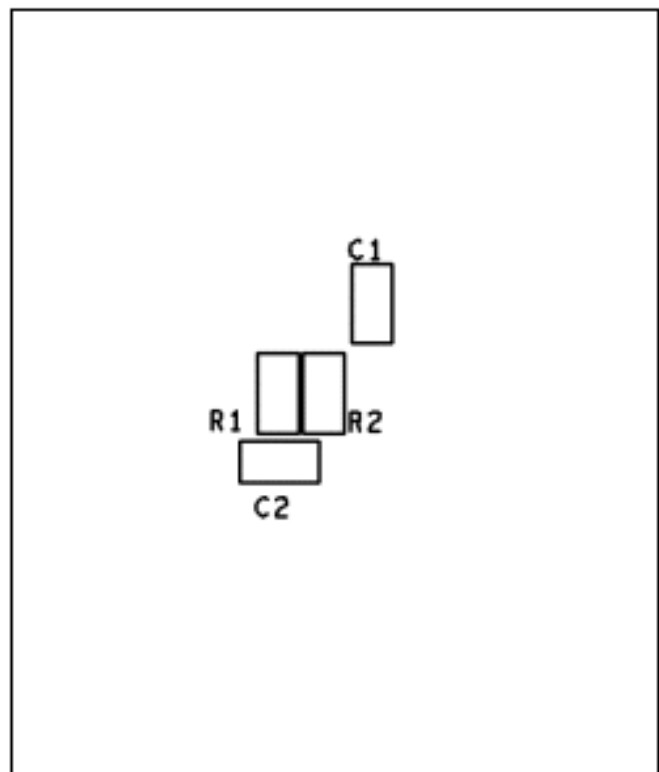


Figure 1.2 E1x1 75Ω impedance -- Silkscreen bottom layer layout (view mirrored)

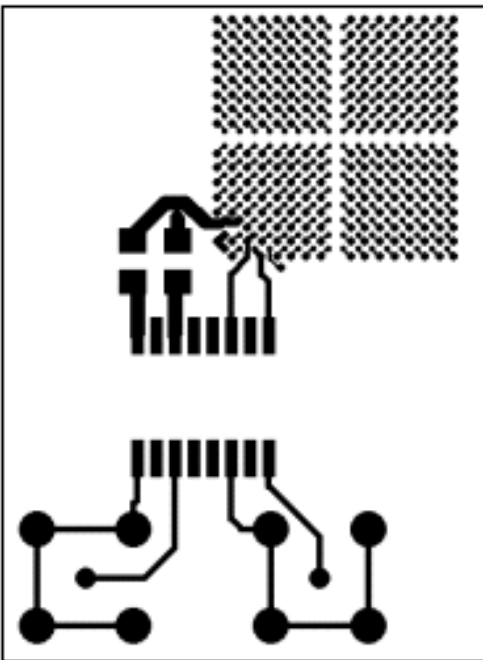


Figure 1.3 E1x1 75Ω impedance -- Top conducting layer layout

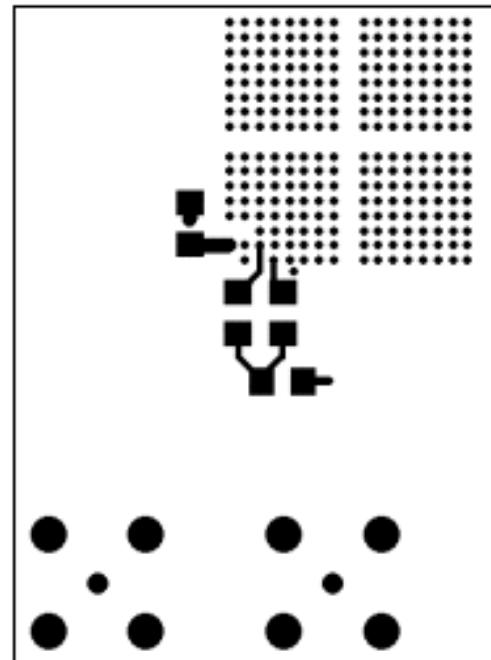


Figure 1.4 E1x1 75Ω impedance -- Bottom conducting layer layout

2. The layout of a single T1 port interfacing to RJ48 connector with 100Ω impedance. All figures

are twice the actual size.

Table 2. Layout Components

| Ref Des | Qty | Description | Supplier | Part Number |
|---------|-----|--|----------------------|---------------|
| C1 | 1 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2 | 1 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1 | 1 | RJ48 8 Pin Single Port Connector | Molex | 15-43-8588 |
| R1, R2 | 2 | Resistor 1206 60.4W 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| T1 | 1 | Transformer, 1CT to 1CT & 1CT to 2CT, 16P SMT | Pulse | T1094 |
| U1 | 1 | Octal Transceiver 0-70C 256P BGA | Dallas Semiconductor | DS26528 |

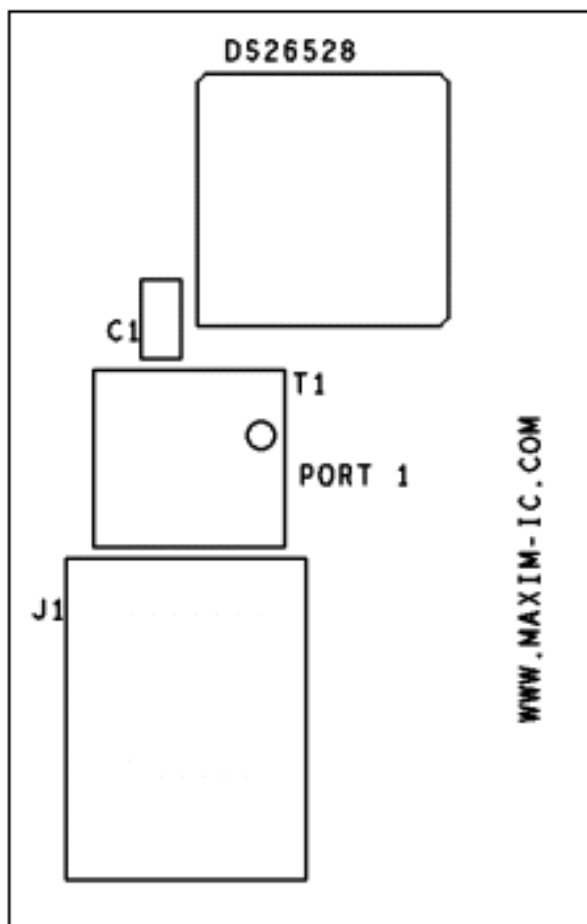


Figure 2.1 T1x1 100Ω impedance -- Silkscreen top layer layout

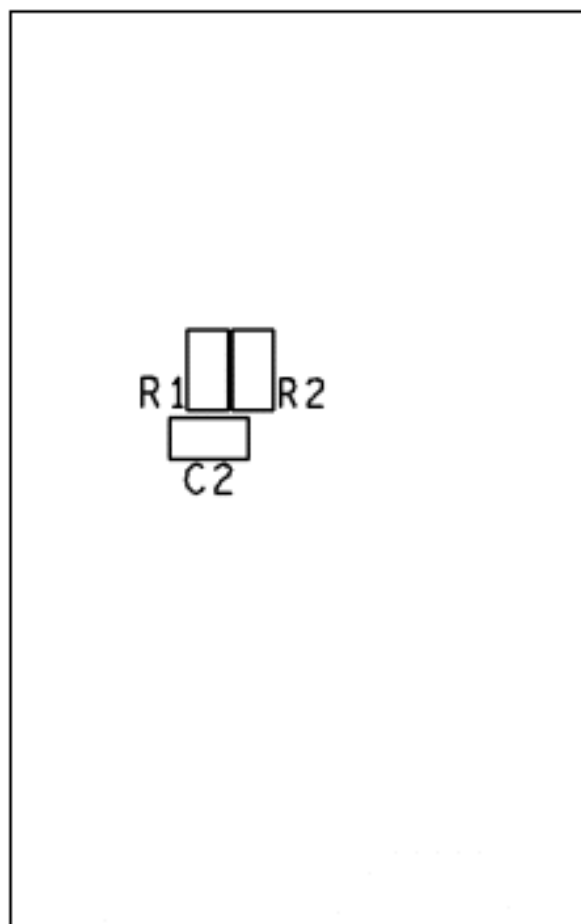


Figure 2.2 T1x1 100Ω impedance -- Silkscreen bottom layer layout (view mirrored)

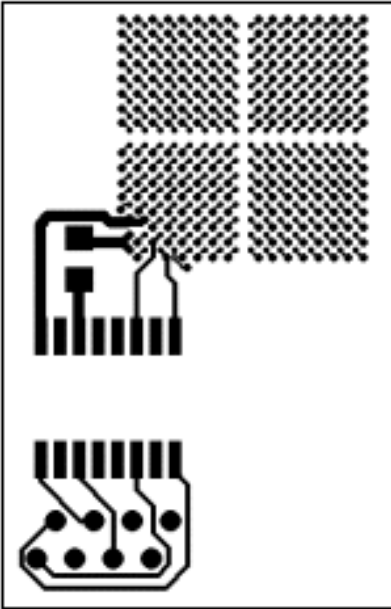


Figure 2.3 T1x1 100Ω impedance --
Top conducting layer layout

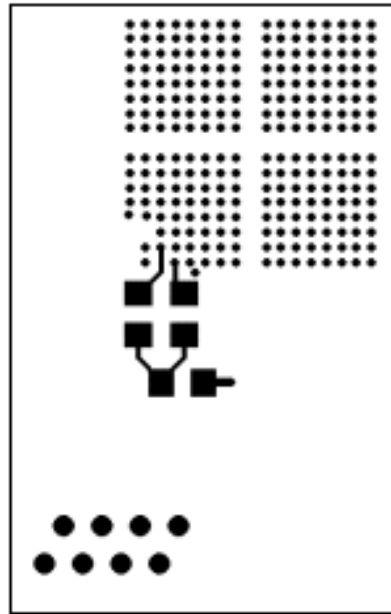


Figure 2.4 T1x1 100Ω impedance --
Bottom conducting layer layout

3. The layout of a single E1 port interfacing to RJ45 connector with 120Ω impedance. All figures are twice the actual size.

Table 3. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|--------|-----|---|----------------------|----------------|
| C1 | 1 | 1206 Ceram 1uF 16v 10% | Panasonic | ECJ-3YB1C105K |
| C2 | 1 | 1206 Ceram .1uF 50v 10% | Panasonic | ECJ-3VB1H104K |
| J1 | 1 | RJ48 8 pin single port connector | Molex | 15-43-8588 |
| R1, R2 | 2 | Resistor 1206 60.4Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| R3, R4 | 2 | Resistor 1206 0Ω 1/8W 5% | Panasonic | ERJ-8GEYJ0R00V |
| T1 | 1 | Transformer, 1CT_1CT & 1CT_2CT, 16P SMT | Pulse | T1094 |
| U1 | 1 | Octal Transceiver 0-70c 256p BGA | Dallas Semiconductor | DS26528 |

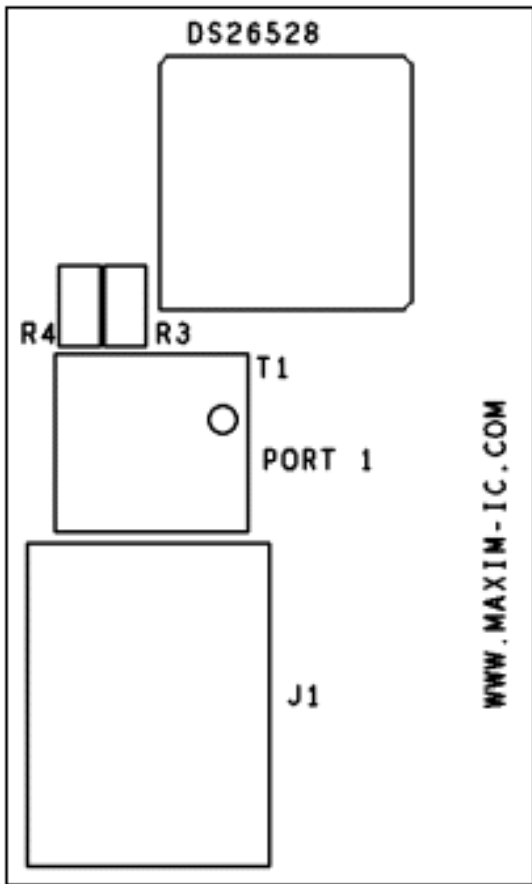


Figure 3.1 E1x1 120Ω impedance
-- Silkscreen top layer layout

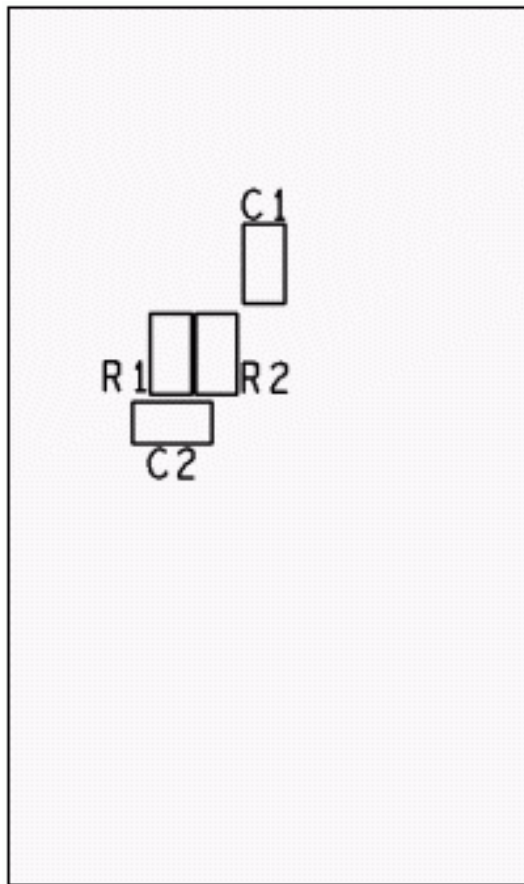


Figure 3.2 E1x1 120Ω impedance
-- Silkscreen bottom layer layout
(view mirrored)

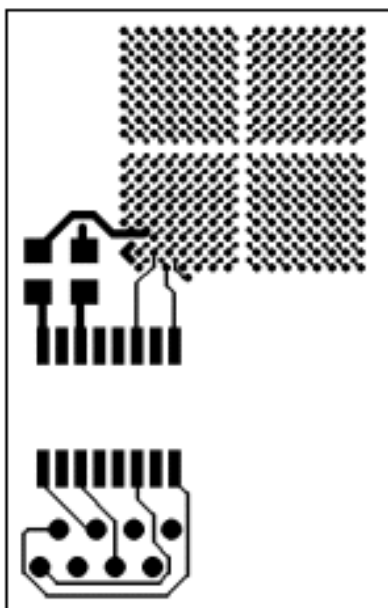


Figure 3.3 E1x1 120Ω impedance
-- Top conducting layer layout

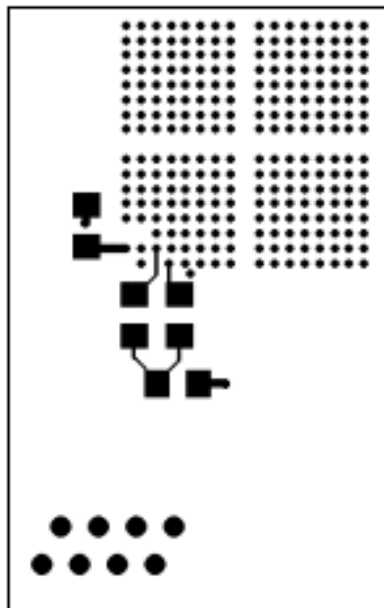


Figure 3.4 E1x1 120Ω impedance
-- Bottom conducting layer layout

4. The layout of four E1 ports interfacing to BNC connectors with 75Ω impedance. All figures are actual size.

Table 4. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|-------------------------|-----|--|----------------------|----------------|
| C1, C3, C5, C7 | 4 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2, C4, C6, C8 | 4 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1, J3, J5, J6 | 4 | Connector BNC 75Ω RA 5 Pin | Trompetor | UCBJR22 |
| J2, J4, J7, J8 | 4 | Connector BNC 75Ω Vertical 5Pin | Cambridge | CP-BNCPC-004 |
| R1, R2, R5, R6, R9-R12 | 8 | Resistor 1206 60.4Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| R3, R4, R7, R8, R13-R16 | 8 | Resistor 1206 0Ω 1/8W 5% | Panasonic | ERJ-8GEYJ0R00V |
| T1 | 1 | Transformer, XMIT/RCV, 1 to 2 & 1 to 1, SMT 32 Pin | Pulse | TX1475 |
| U1 | 1 | Octal Transceiver 0-70C 256P BGA | Dallas Semiconductor | DS26528 |

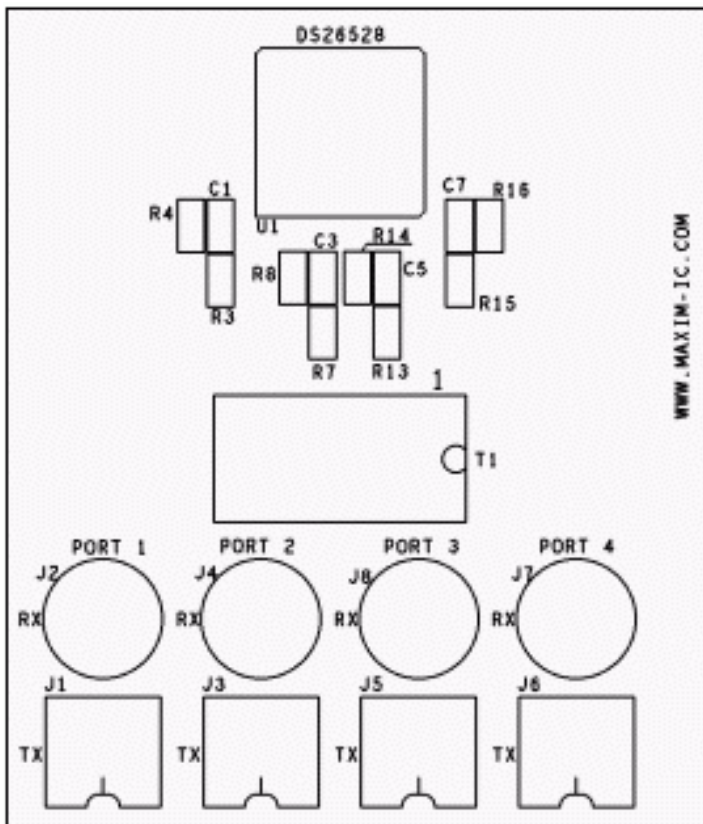


Figure 4.1 E1x4 75Ω impedance -- Silkscreen top layer layout

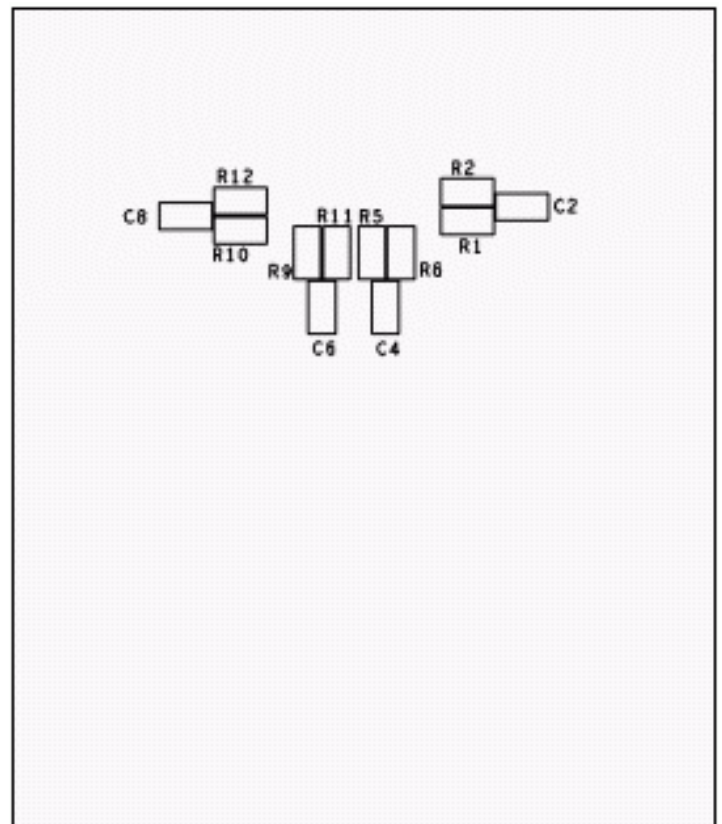


Figure 4.2 E1x4 75Ω impedance -- Silkscreen bottom layer layout (view

mirrored)

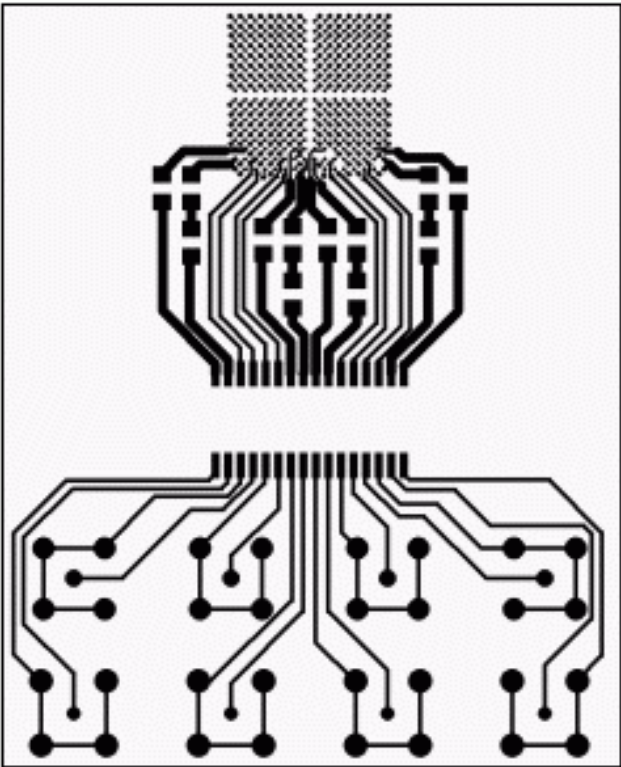


Figure 4.3 E1x4 75Ω impedance -- Top conducting layer layout

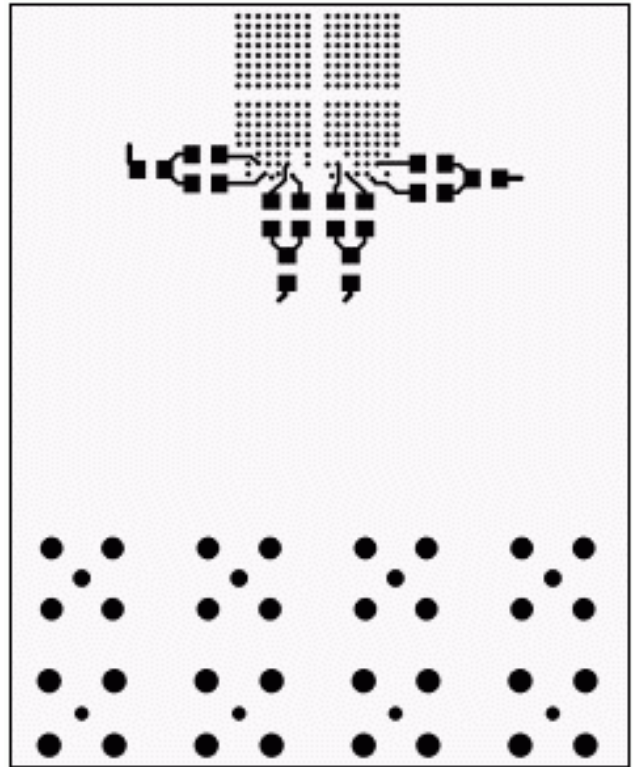


Figure 4.4 E1x4 75Ω impedance -- Bottom conducting layer layout

5. The layout of four T1 ports interfacing to RJ45 connectors with 100Ω impedance. All figures are actual size.

Table 5. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|------------------------|-----|--|----------------------|---------------|
| C1, C3, C5, C7 | 4 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2, C4, C6, C8 | 4 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1 | 1 | RA RJ45 8Pin 4 Port Jack | Molex | 43223-8140 |
| R1, R2, R5, R6, R9-R12 | 8 | Resistor 1206 60.4Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| T1 | 1 | Transformer, XMIT/RCV, 1 to 2 & 1 to 1, SMT 32 Pin | Pulse | TX1475 |
| U1 | 1 | Octal Transceiver 0-70C 256P BGA | Dallas Semiconductor | DS26528 |

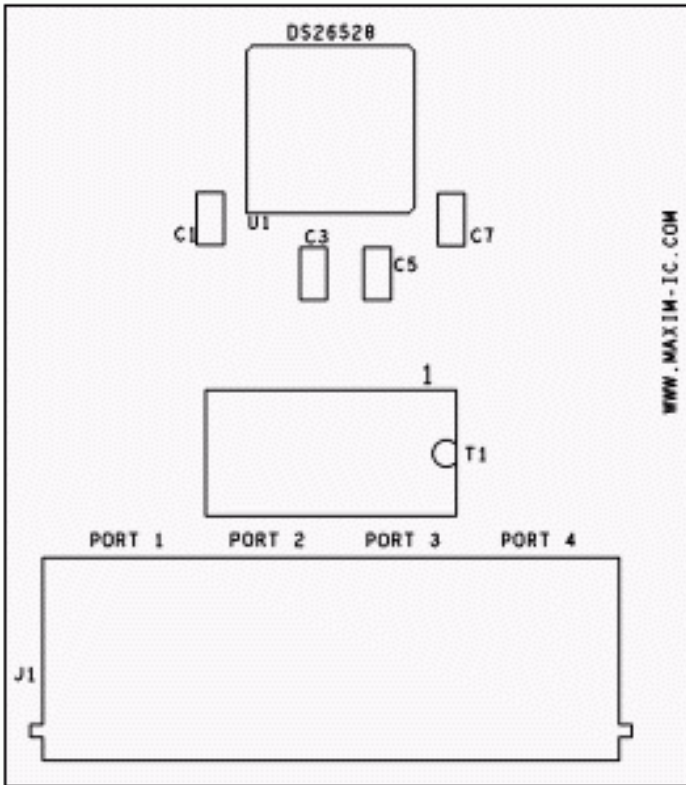


Figure 5.1 T1x4 100Ω impedance -- Silkscreen top layer layout

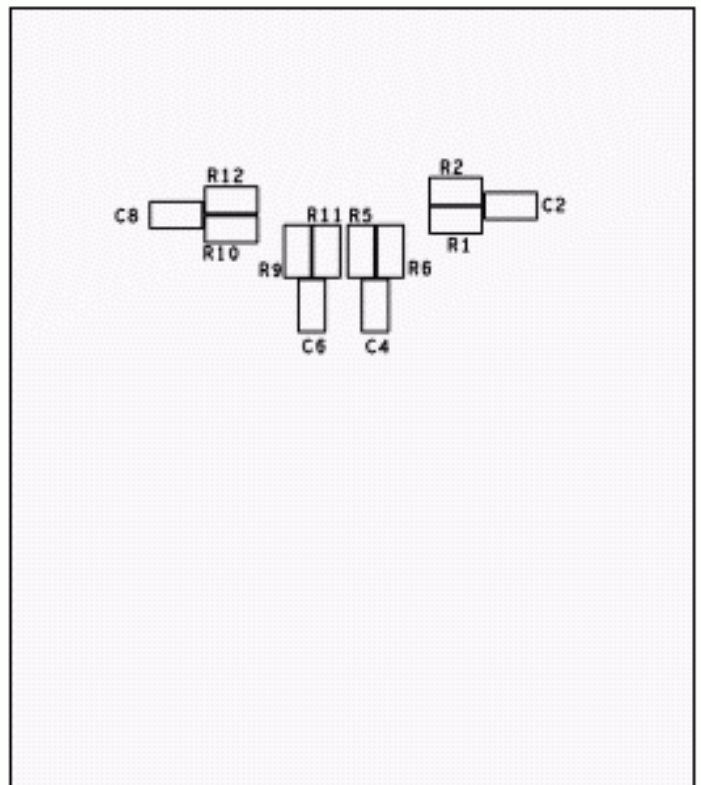


Figure 5.2 T1x4 100Ω impedance -- Silkscreen bottom layer layout (view mirrored)

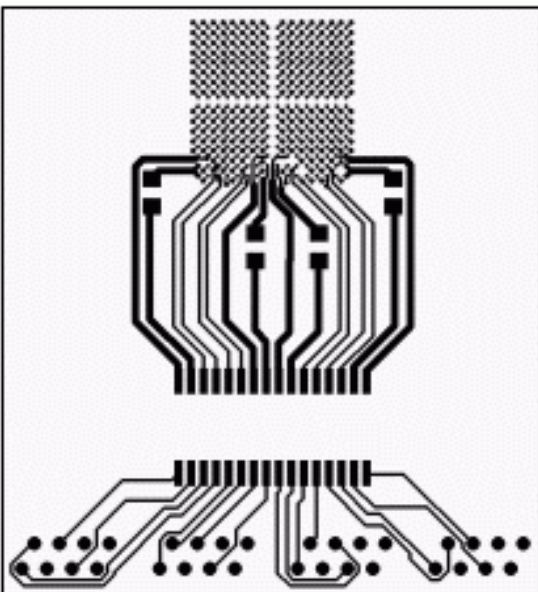


Figure 5.3 T1x4 100Ω impedance -- Top conducting layer layout

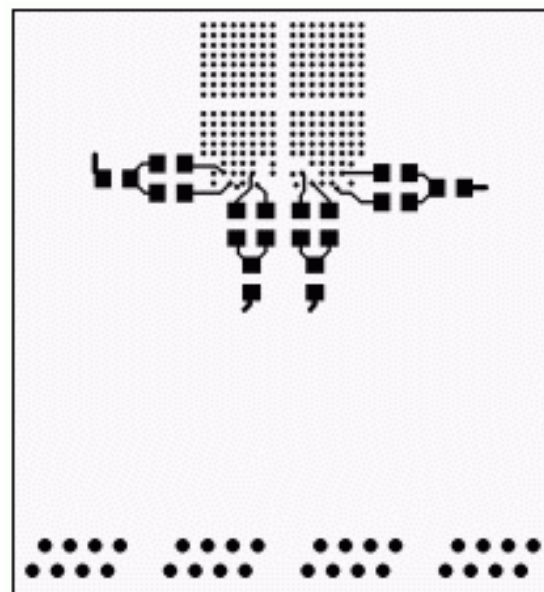


Figure 5.4 T1x4 100Ω impedance -- Bottom conducting layer layout

6. The layout of four E1 ports interfacing to RJ45 connectors with 120Ω impedance. All figures are actual size.

Table 6. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|-------------------------|-----|--|----------------------|----------------|
| C1, C3, C5, C7 | 4 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2, C4, C6, C8 | 4 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1 | 1 | RA RJ45 8Pin 4Port Jack | Molex | 43223-8140 |
| R3, R4, R7, R8, R13-R16 | 8 | Resistor 1206 0 Ω 1/8W 5% | Panasonic | ERJ-8GEYJ0R00V |
| T1 | 1 | Transformer, XMIT/RCV, 1 to 2 & 1 to 1, SMT 32 Pin | Pulse | TX1475 |
| U1 | 1 | Octal Transceiver 0-70C 256P BGA | Dallas Semiconductor | DS26528 |

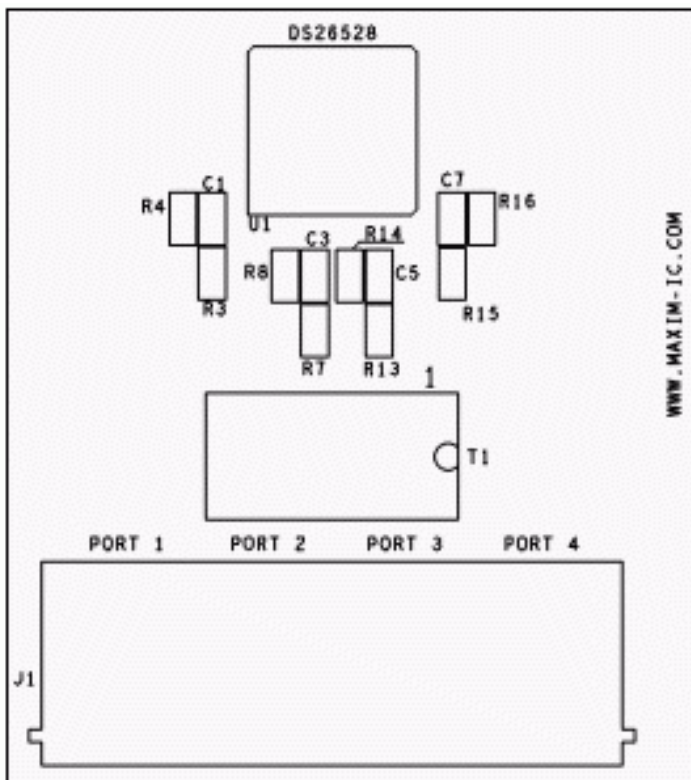


Figure 6.1 E1x4 120 Ω impedance -- Silkscreen top layer layout

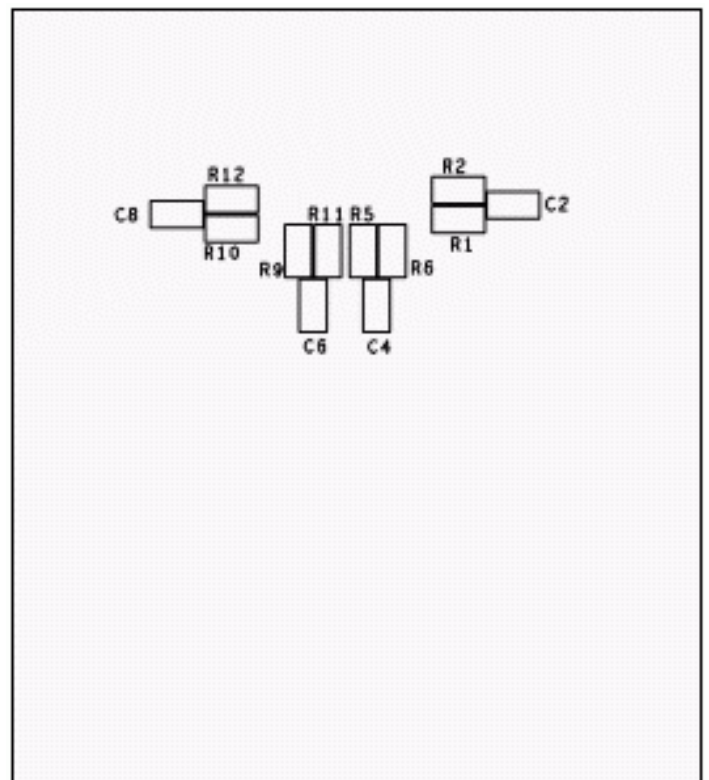


Figure 6.2 E1x4 120 Ω impedance -- Silkscreen bottom layer layout (view mirrored)

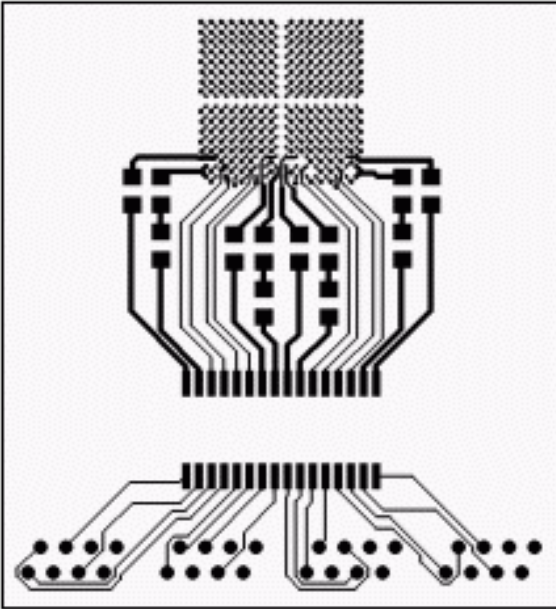


Figure 6.3 E1x4 120 Ω impedance -- Top conducting layer layout

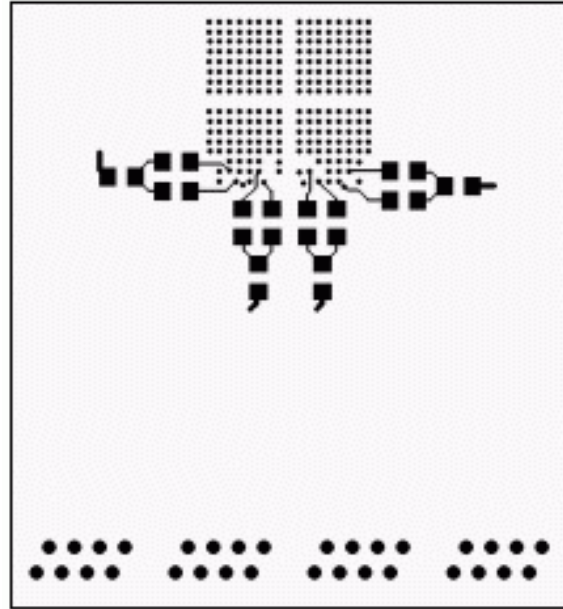


Figure 6.4 E1x4 120 Ω impedance -- Bottom conducting layer layout

7. The layout of eight E1 ports interfacing to BNC connectors with 75 Ω impedance. All figures are actual size.

Table 7. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|--|-----|--|-----------|----------------|
| C1, C3, C5, C7, C9, C11, C13, C15 | 8 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2, C4, C6, C8, C10, C12, C14, C16 | 8 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1, J4, J6, J8, J10, J12, J14, J15 | 8 | Connector BNC 75 Ω Vertical 5 Pin | Cambridge | CP-BNCP-004 |
| J2, J3, J5, J7, J9, J11, J13, J16 | 8 | Connector BNC 75 Ω RA 5 Pin | Trompetor | UCBJR220 |
| R1, R2, R5, R6, R9-R12, R17, R18, R20, R23, R25-R28 | 16 | Resistor 1206 60.4 Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| R3, R4, R7, R8, R13-R16, R19, R21, R22, R24, R29-R32 | 16 | Resistor 1206 0W 1/8 Ω 5% | Panasonic | ERJ-8GEYJ0R00V |
| T1, T2 | 2 | Transformer, XMIT/RCV, 1 to 2 & 1 to 1, SMT 32 PIN | Pulse | TX1475 |

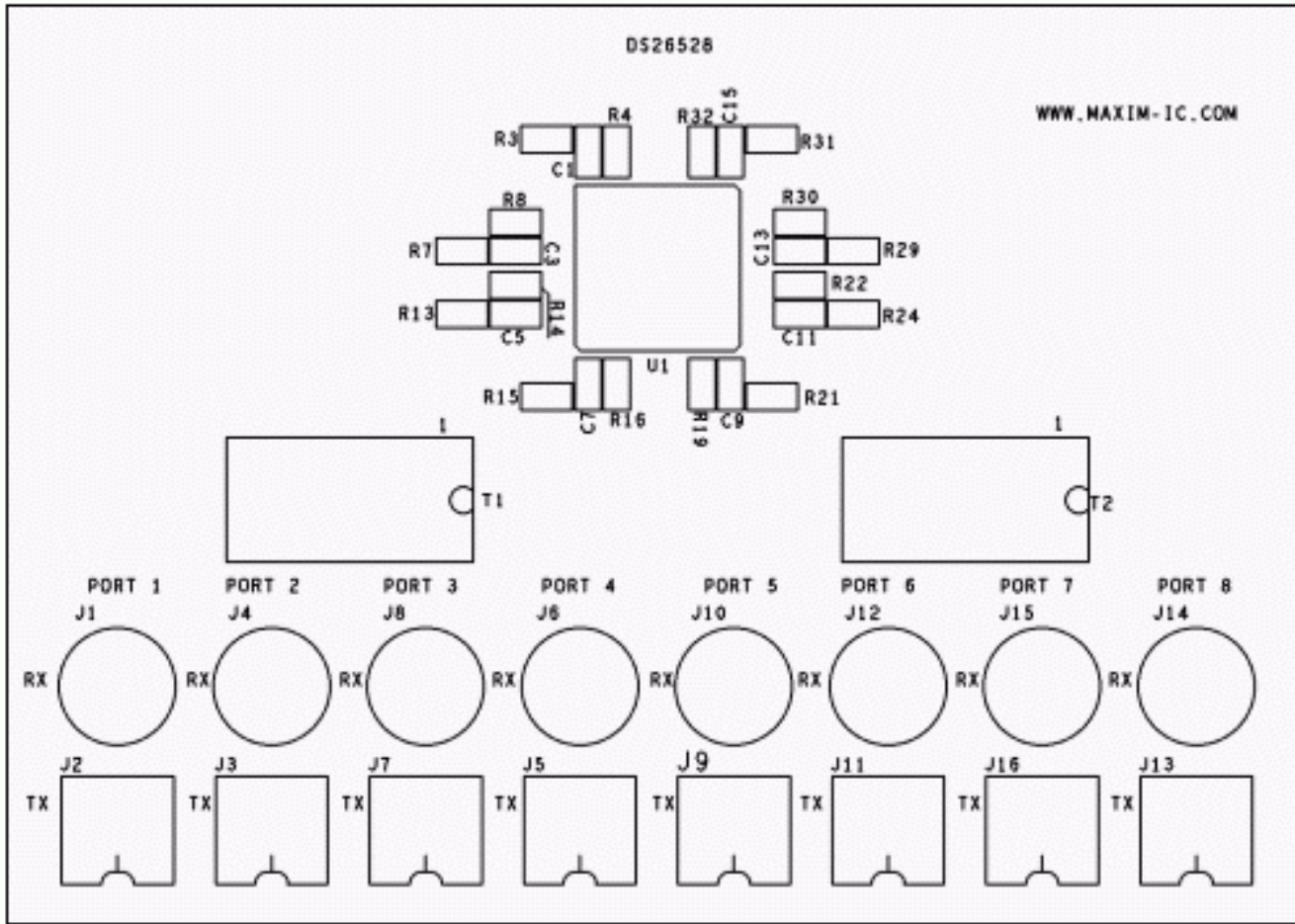


Figure 7.1 E1x8 75Ω impedance -- Silkscreen top layer layout

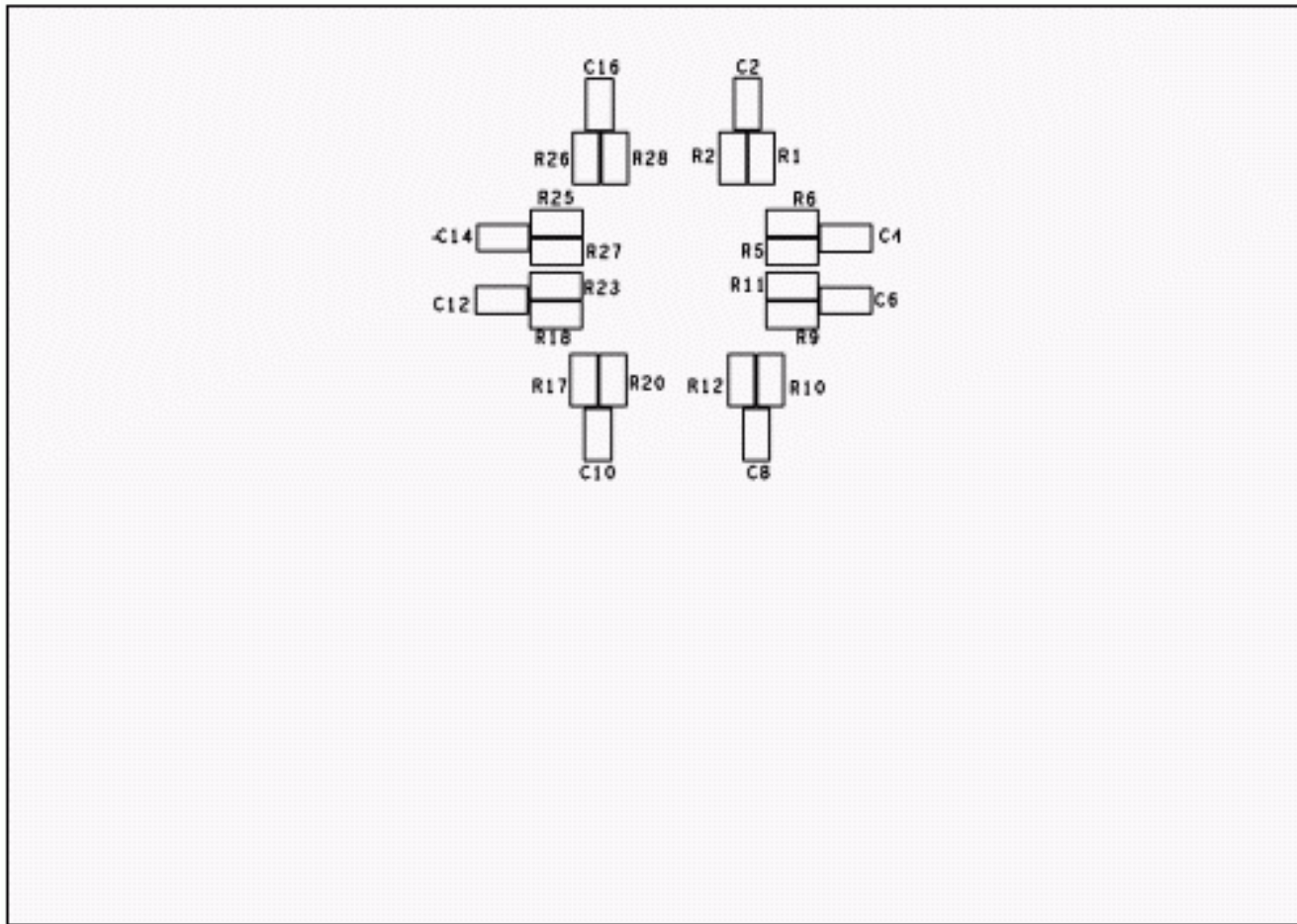


Figure 7.2 E1x8 75 Ω impedance -- Silkscreen bottom layer layout (view mirrored)

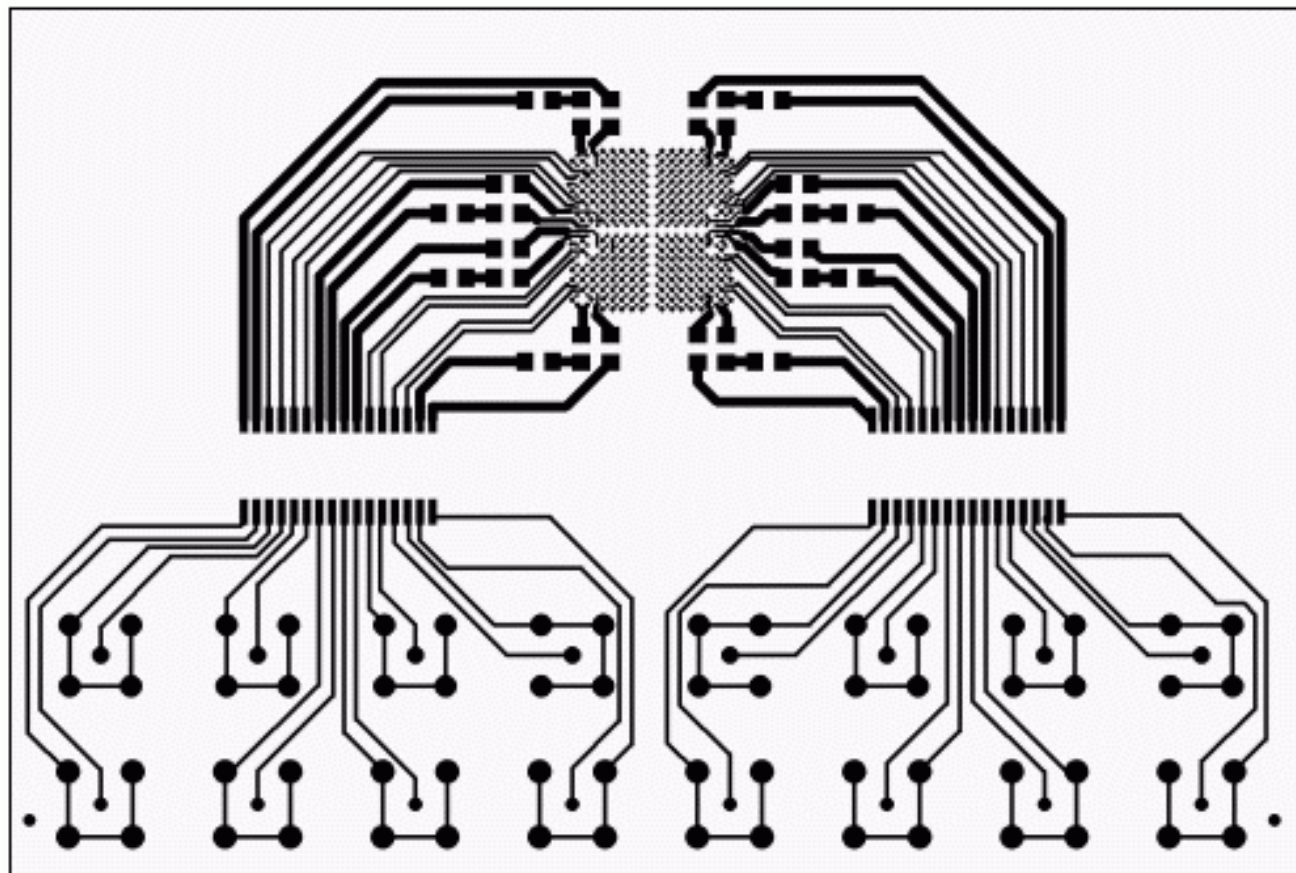


Figure 7.3 E1x8 75 Ω impedance -- Top conducting layer layout

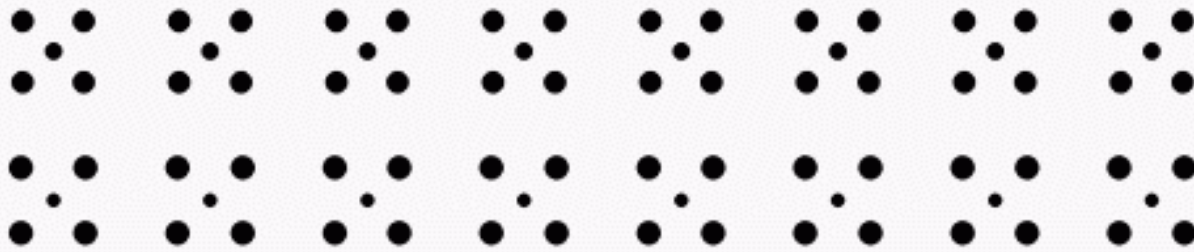
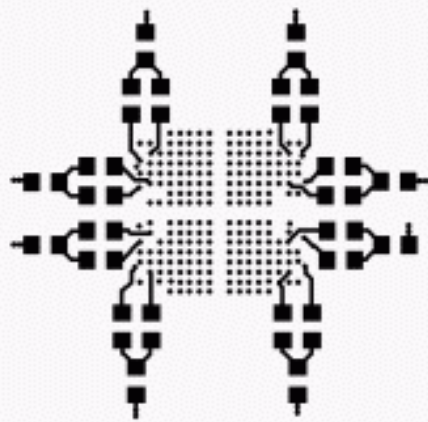


Figure 7.4 E1x8 75 Ω impedance -- Bottom conducting layer layout

8. The layout of eight T1 ports interfacing to RJ45 connectors with 100 Ω impedance. All figures are actual size.

Table 8. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|---|-----|--|-----------|---------------|
| C1, C3, C5, C7, C9, C11, C13, C15 | 8 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2, C4, C6, C8, C10, C12, C14, C16 | 8 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1, J2 | 2 | RA RJ45 8Pin 4 Port Jack | Molex | 43223-8140 |
| R1, R2, R5, R6, R9-R12, R17, R18, R20, R23, R25-R28 | 16 | Resistor 1206 60.4 Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| T1, T2 | 2 | Transformer, XMIT/RCV, 1 to 2 & 1 to 1, SMT 32 Pin | Pulse | TX1475 |

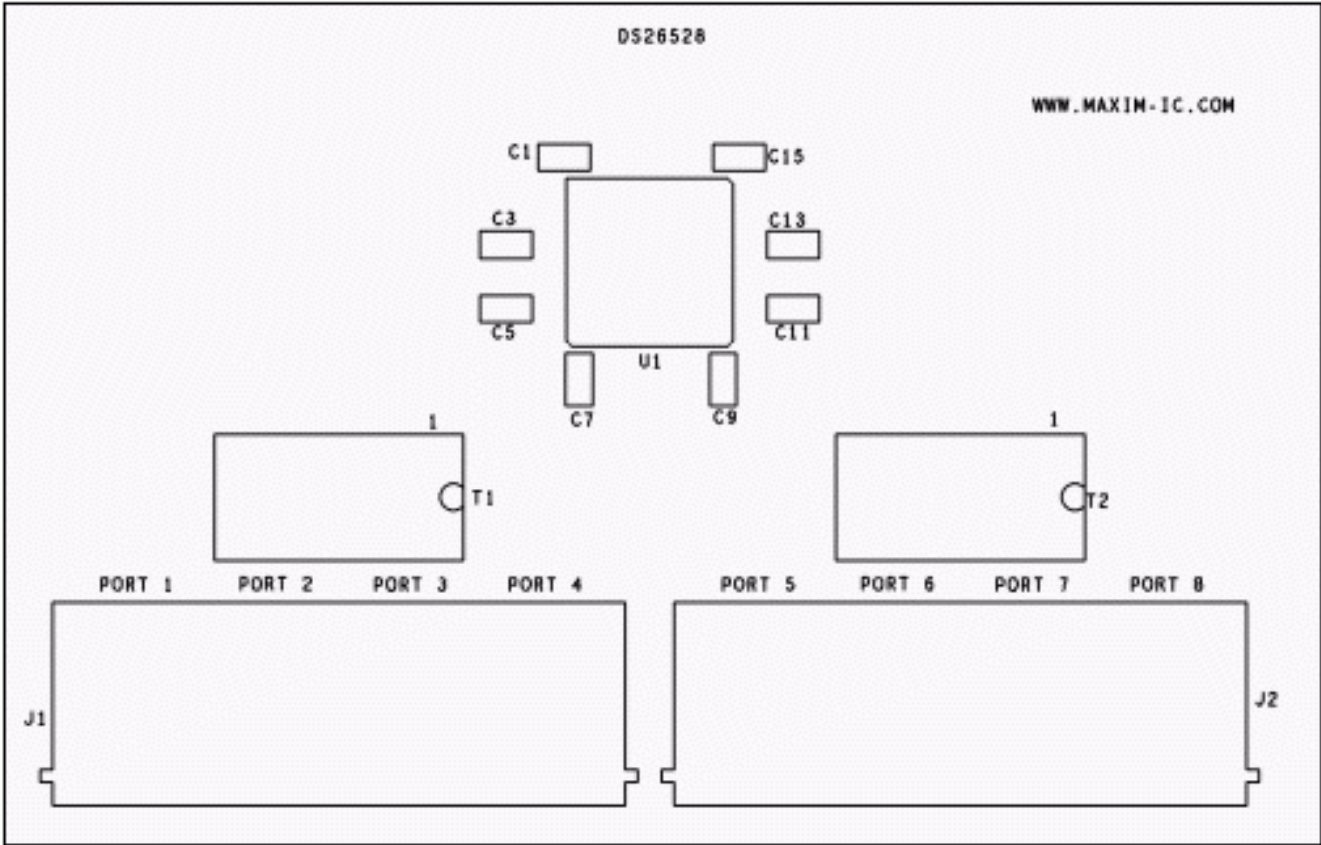


Figure 8.1 T1x8 100Ω impedance -- Silkscreen top layer layout

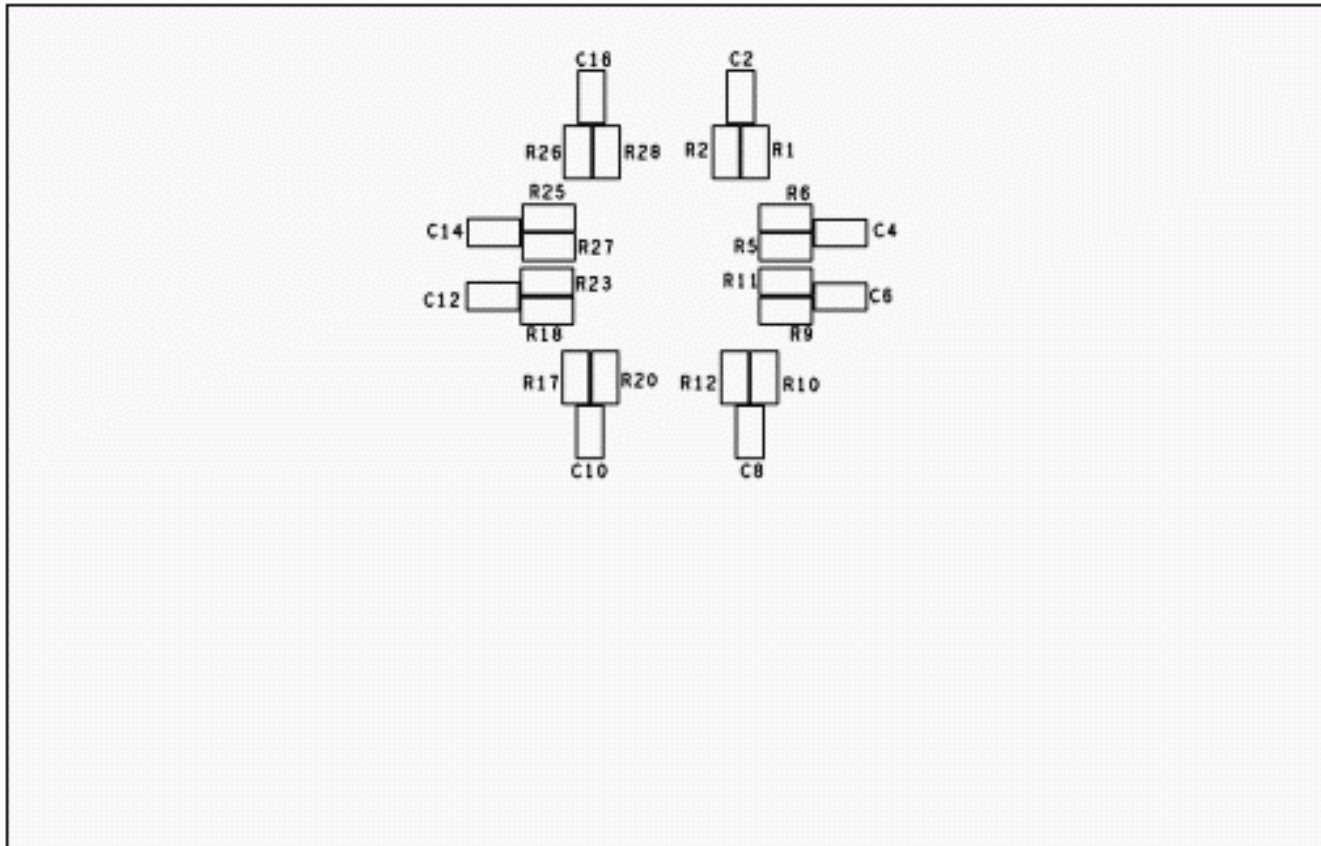


Figure 8.2 T1x8 100Ω impedance -- Silkscreen bottom layer layout (view mirrored)

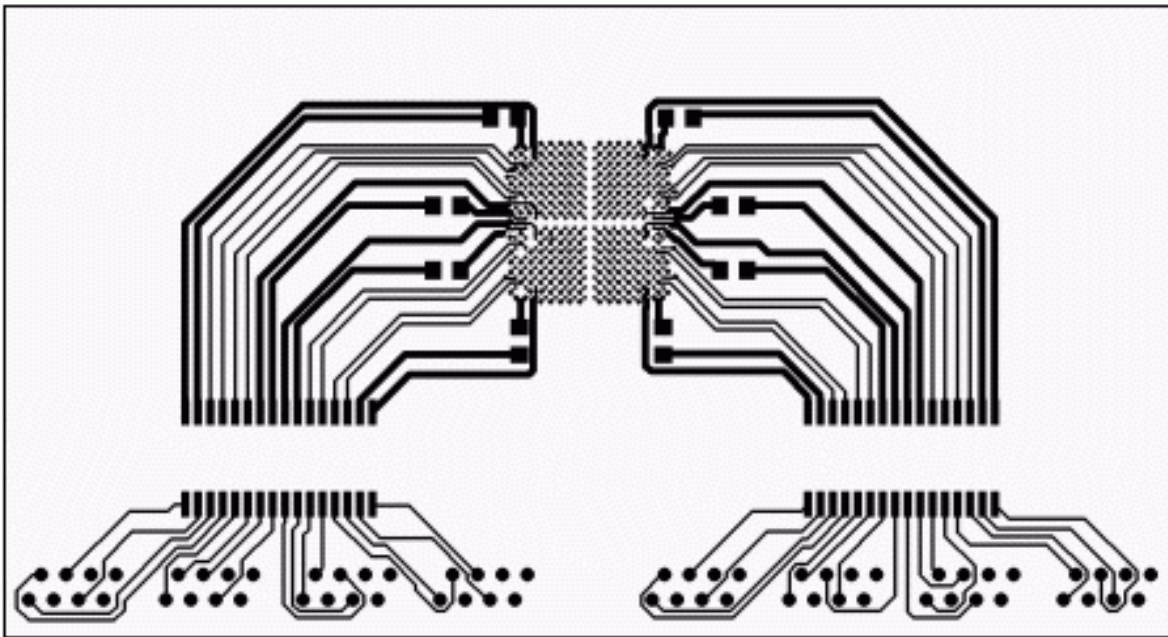


Figure 8.3 T1x8 100Ω impedance -- Top conducting layer layout

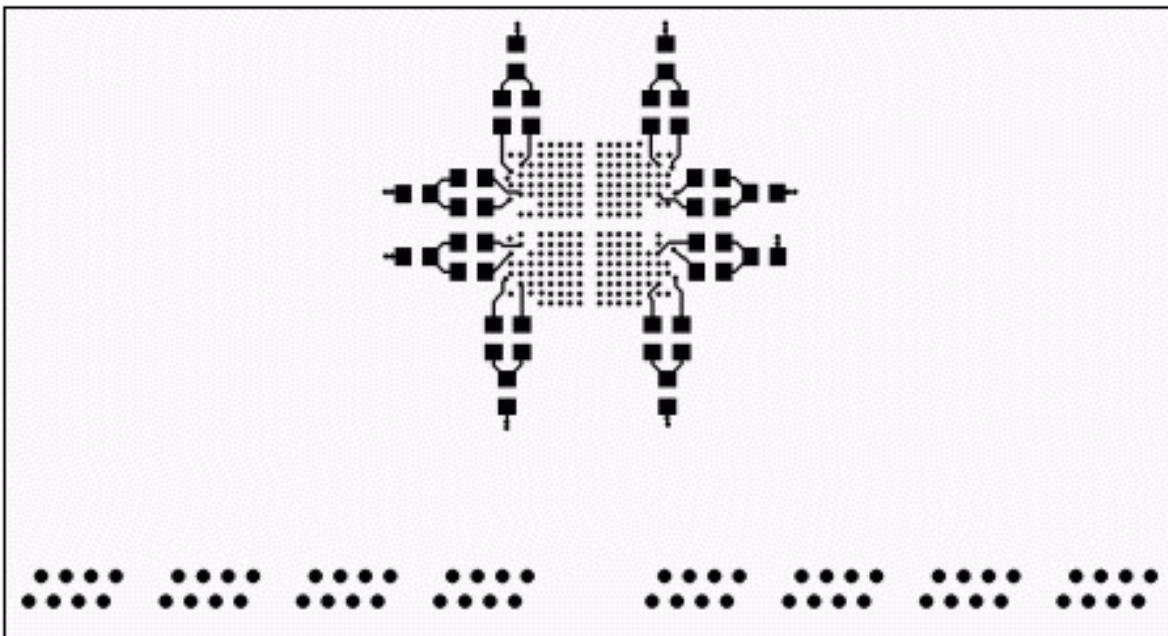


Figure 8.4 T1x8 100Ω impedance -- Bottom conducting layer layout

9. The layout of eight E1 ports interfacing to RJ45 connectors with 120Ω impedance. All figures are actual size.

Table 9. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|------|-----|-------------|----------|-------------|
|------|-----|-------------|----------|-------------|

| | | | | |
|--|----|--|----------------------|----------------|
| C1, C3, C5, C7, C9, C11, C13, C15 | 8 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2, C4, C6, C8, C10, C12, C14, C16 | 8 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J1, J2 | 2 | RA RJ45 8Pin 4 Port Jack | Molex | 43223-8140 |
| R1, R2, R5, R6, R9-R12, R17, R18, R20, R23, R25-R28 | 16 | Resistor 1206 60.4 Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| R3, R4, R7, R8, R13-R16, R19, R21, R22, R24, R29-R32 | 16 | Resistor 1206 0 Ω 1/8W 5% | Panasonic | ERJ-8GEYJ0R00V |
| T1, T2 | 2 | Transformer, XMIT/RCV, 1 to 2 & 1 to 1, SMT 32 Pin | Pulse | TX1475 |
| U1 | 1 | Octal Transceiver 0-70C 256P BGA | Dallas Semiconductor | DS26528 |

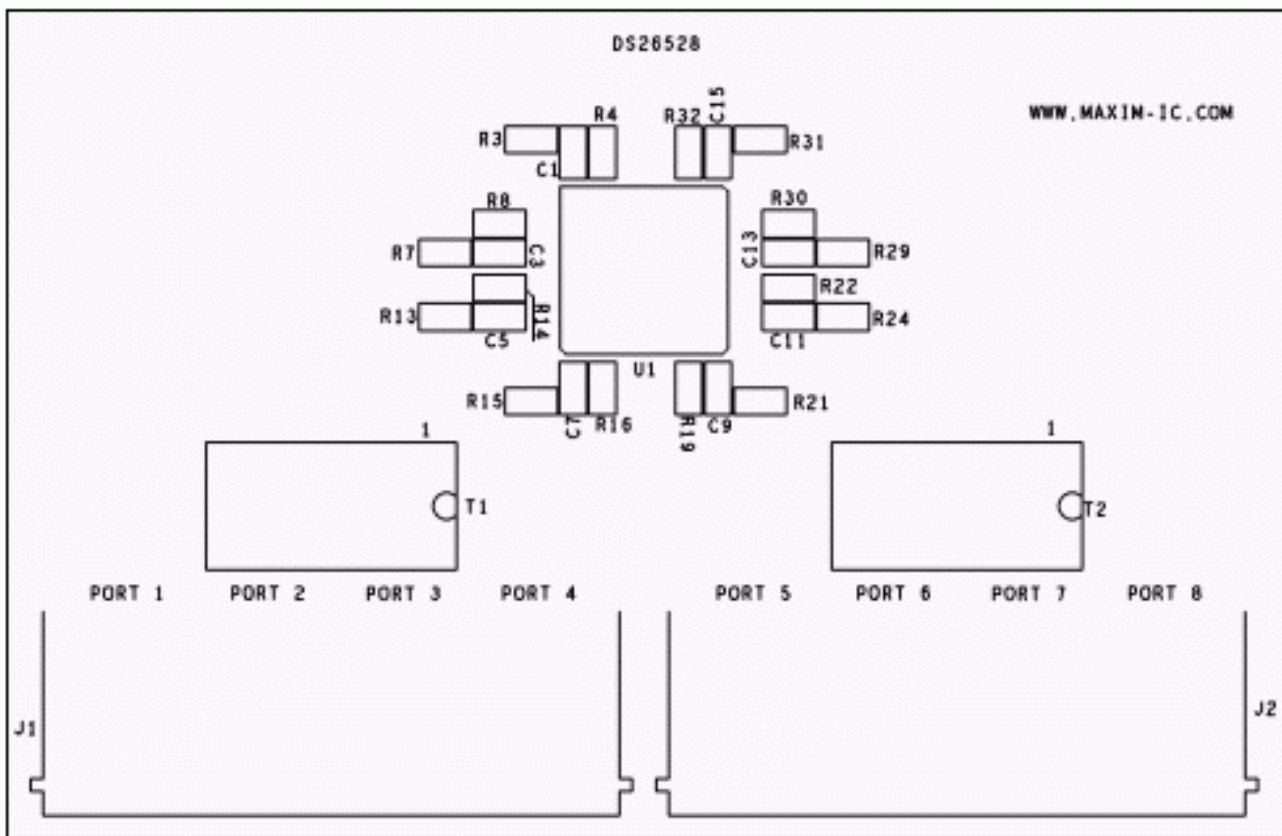


Figure 9.1 E1x8 120 Ω impedance -- Silkscreen top layer layout

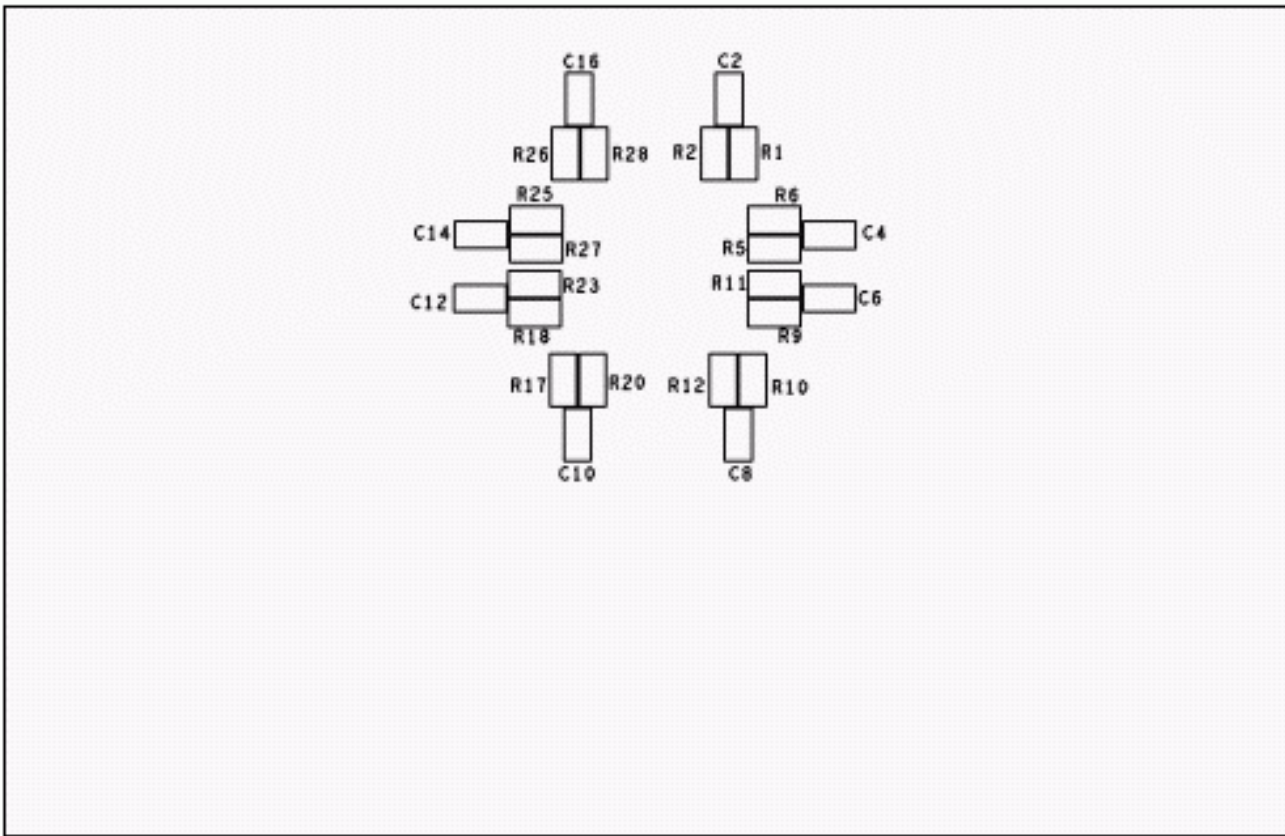


Figure 9.2 E1x8 120 Ω impedance -- Silkscreen bottom layer layout (view mirrored)

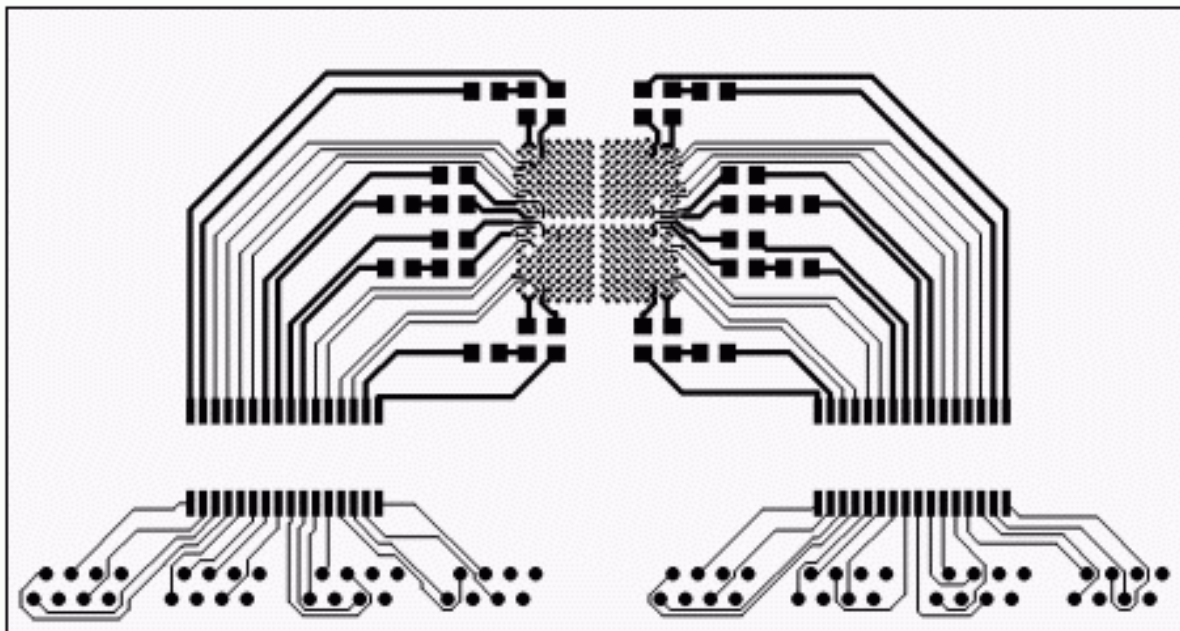


Figure 9.3 E1x8 120 Ω impedance -- Top conducting layer layout

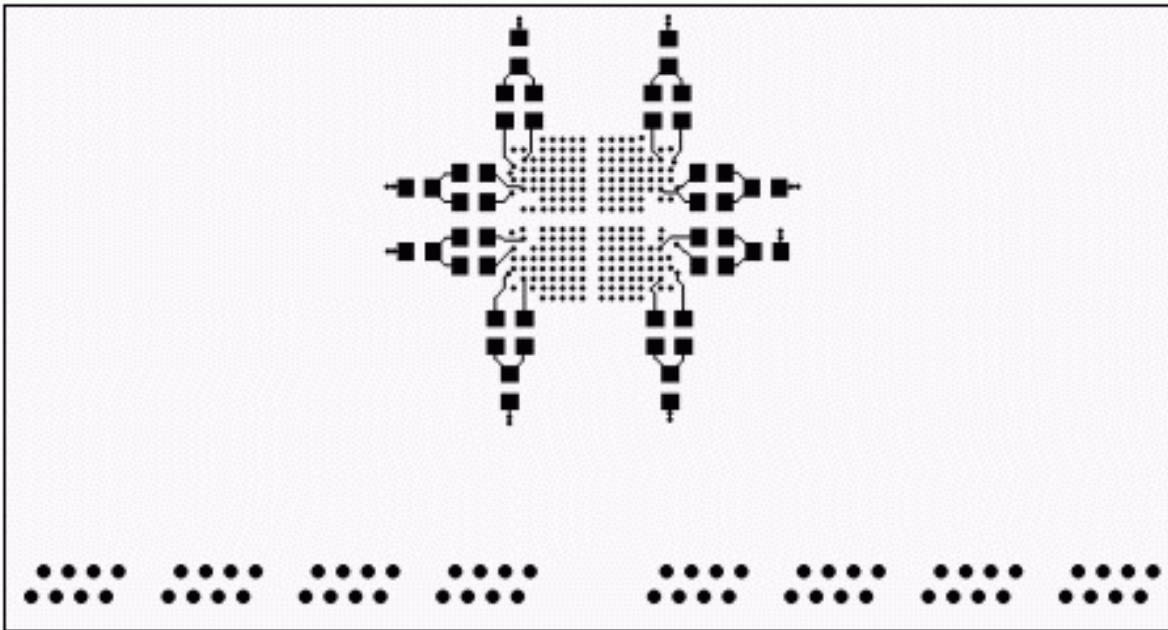


Figure 9.3 E1x8 120 Ω impedance -- Bottom conducting layer layout

10. The interfacing layout of four T1 ports to RJ45 connectors with 100 Ω impedance and four E1 ports to BNC connectors with 75 Ω impedance. All figures are actual size.

Table 10. Layout Components

| Name | Qty | Description | Supplier | Part Number |
|---|-----|---|----------------------|----------------|
| C1, C3, C5, C7, C9, C11, C13, C15 | 8 | 1206 Ceram 1uF 16V 10% | Panasonic | ECJ-3YB1C105K |
| C2, C4, C6, C8, C10, C12, C14, C16 | 8 | 1206 Ceram .1uF 50V 10% | Panasonic | ECJ-3VB1H104K |
| J10, J12, J14, J15 | 4 | Connector BNC 75 Ω Vertical 5 Pin | Cambridge | CP-BNCP-004 |
| J9, J11, J13, J16 | 4 | Connector BNC 75 Ω RA 5 Pin | Trompetor | UCBJR220 |
| R1, R2, R5, R6, R9-R12, R17, R18, R20, R23, R25-R28 | 16 | Resistor 1206 60.4 Ω 1/8W 1% | Panasonic | ERJ-8ENF60R4V |
| R19, R21, R22, R24, R29-R32 | 8 | Resistor 1206 0 Ω 1/8W 5% | Panasonic | ERJ-8GEYJ0R00V |
| T1, T2 | 2 | Transformer, XMIT/RCV, 1 to 2 & 1 to 1 SMT 32 Pin | Pulse | TX1475 |
| U1 | 1 | Octal Transceiver 0-70C 256P BGA | Dallas Semiconductor | DS26528 |

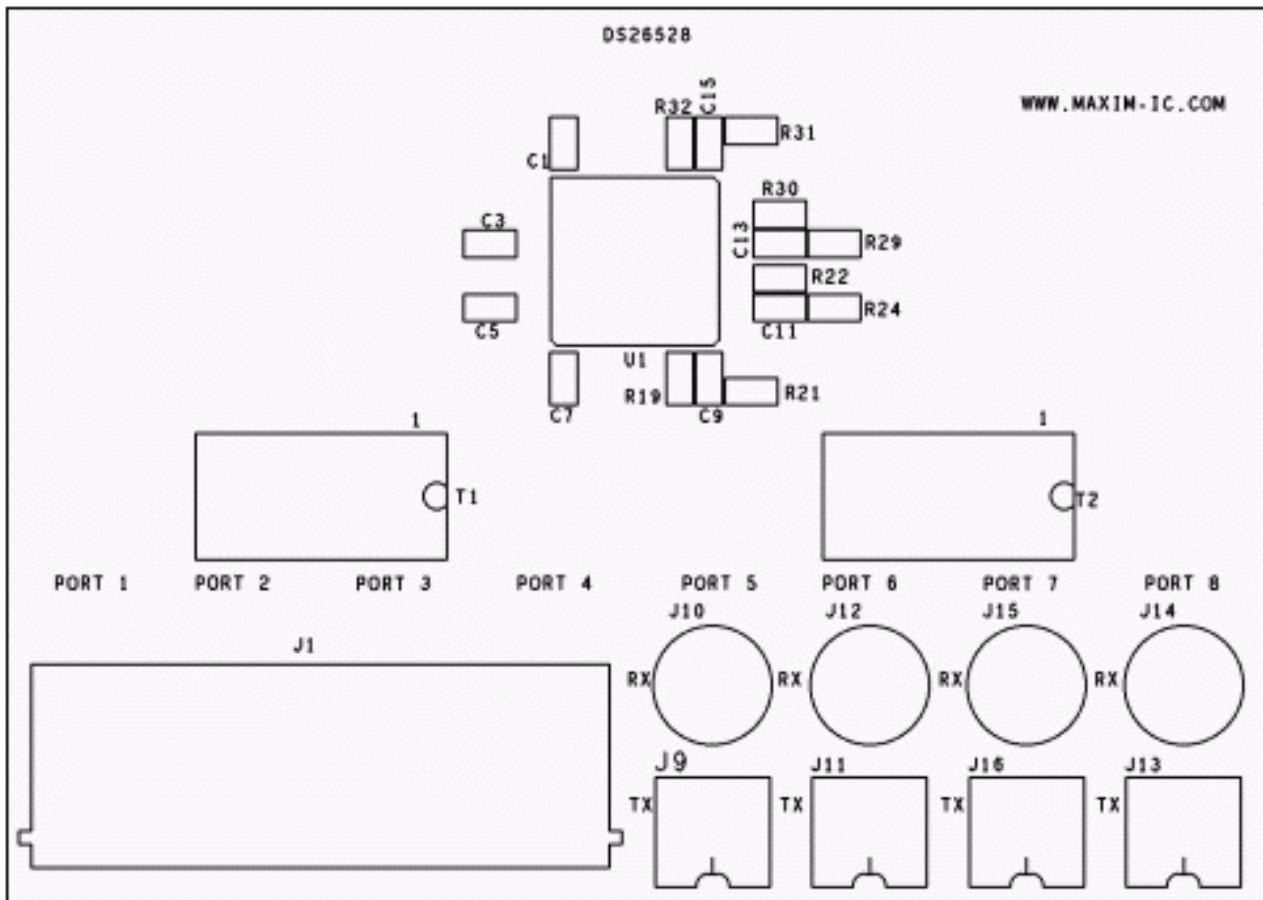


Figure 10.1 T1x4 (Ports 1-4) 100Ω and E1x4 (Ports 5-8) 75Ω impedance -- Silkscreen top layer layout

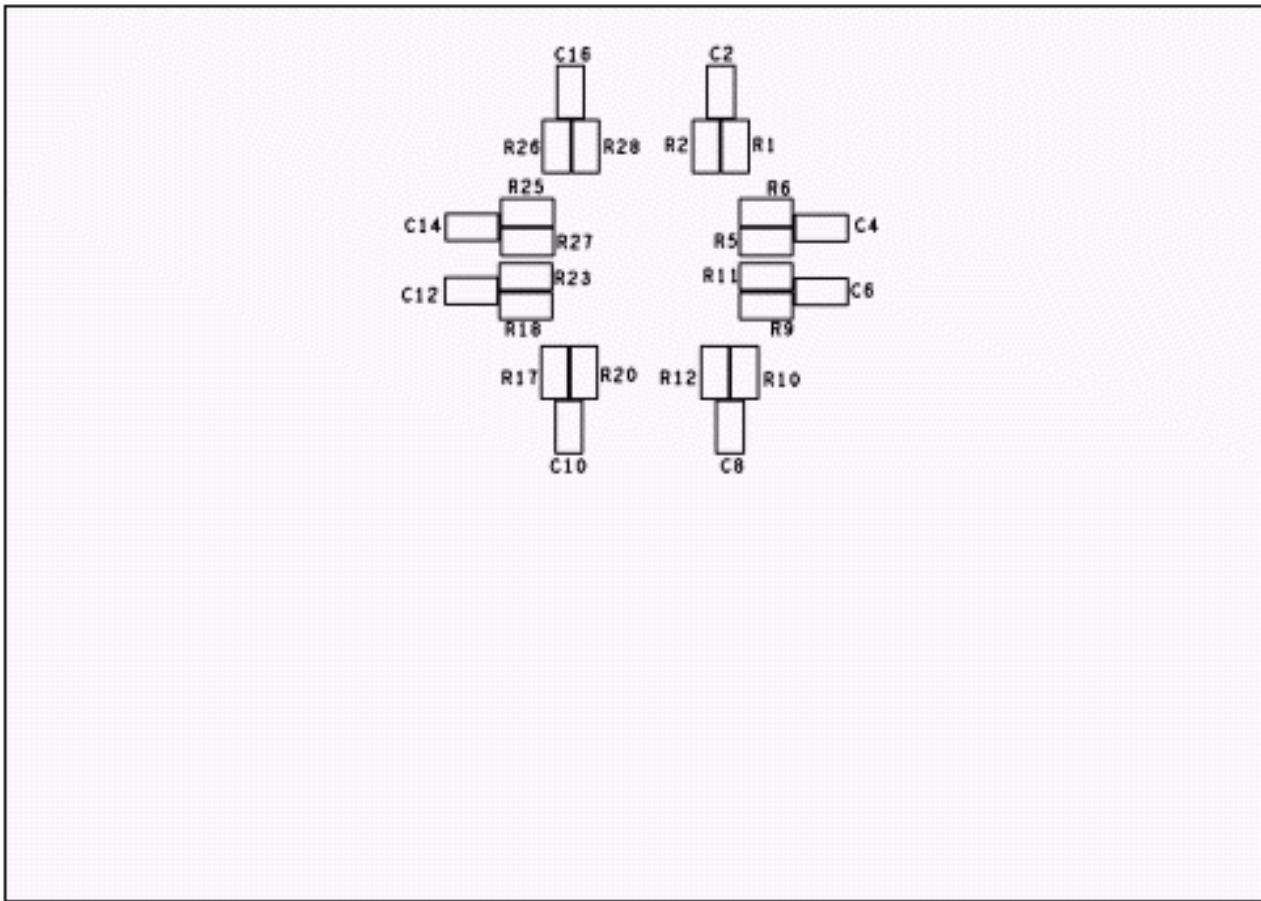


Figure 10.2 T1x4 (Ports 1-4) 100Ω and E1x4 (Ports 5-8) 75Ω impedance -- Silkscreen bottom layer layout (view mirrored)

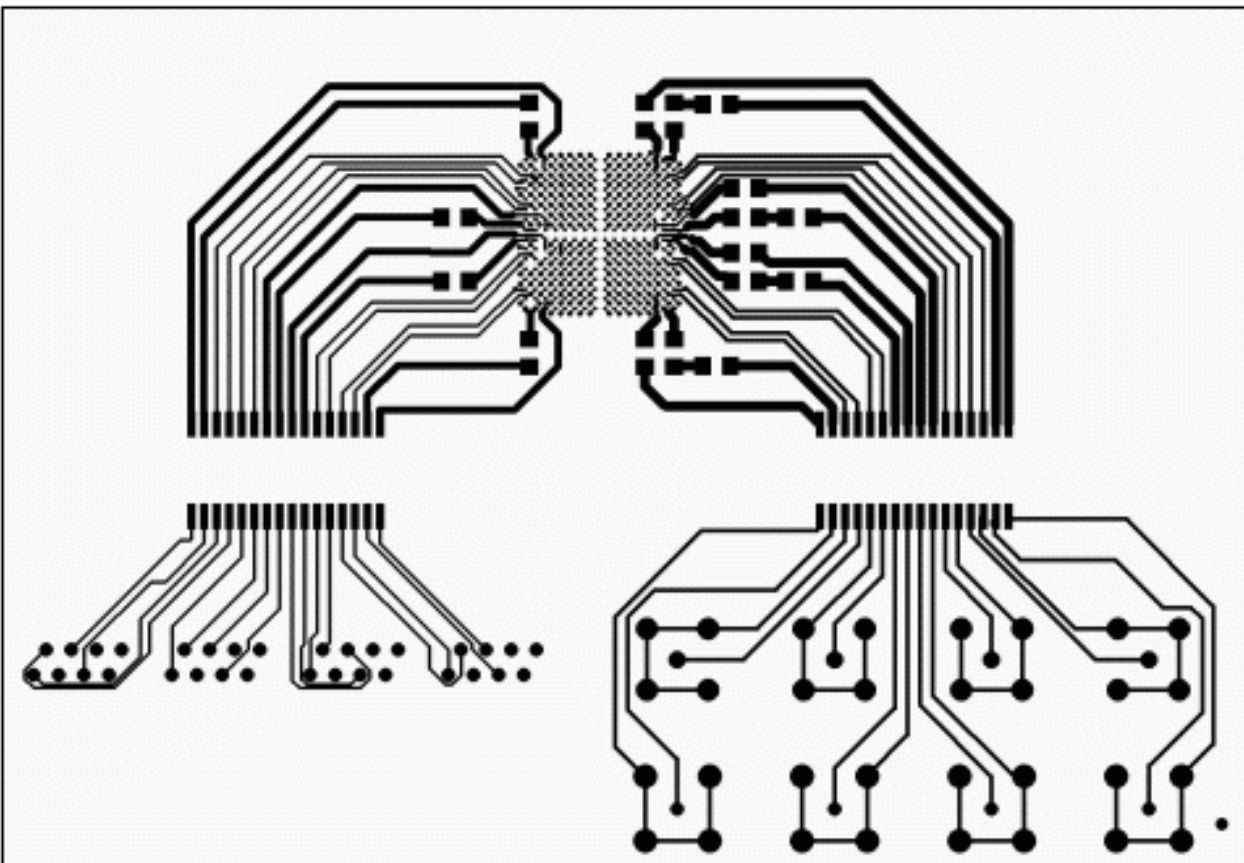


Figure 10.3 T1x4 (Ports 1-4) 100Ω and E1x4 (Ports 5-8) 75Ω impedance -- Top conducting layer

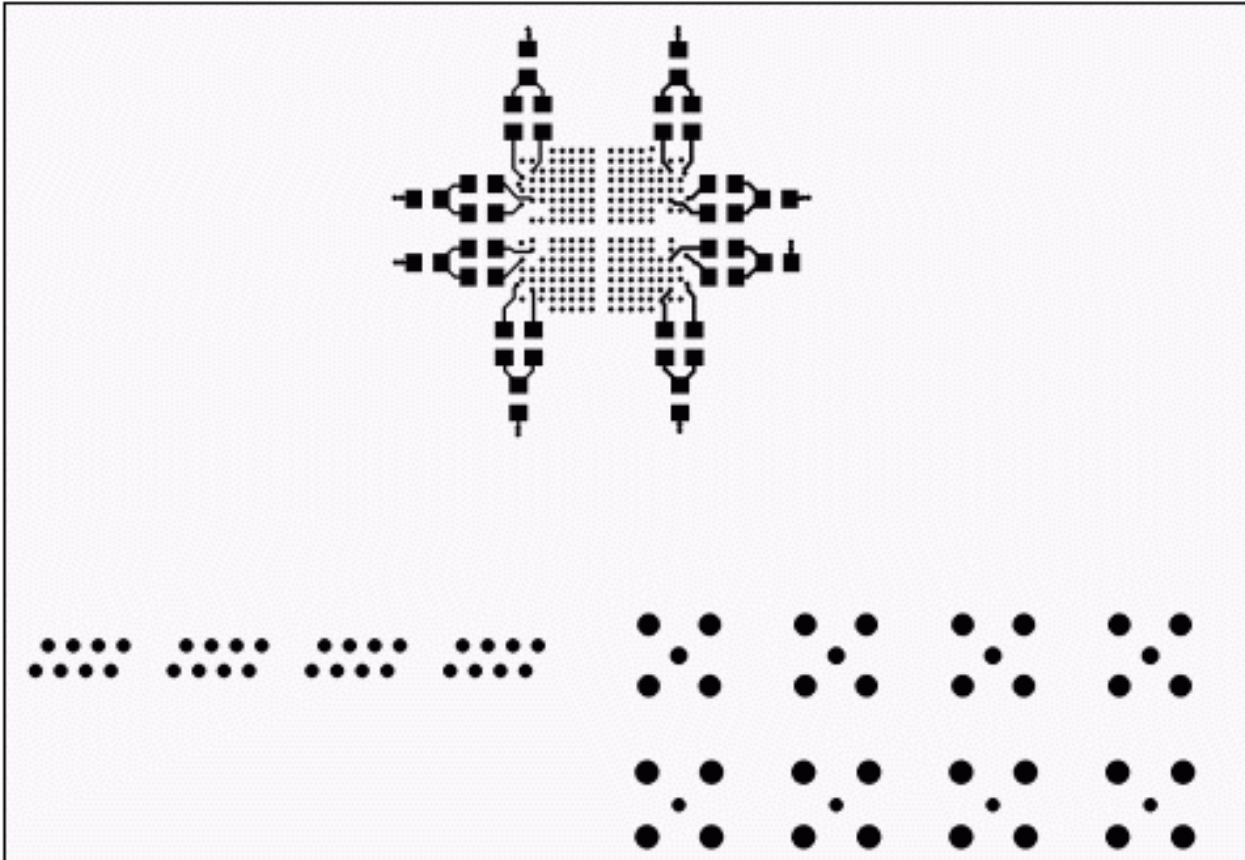


Figure 10.4 T1x4 (Ports 1-4) 100 Ω and E1x4 (Ports 5-8) 75 Ω impedance -- Bottom conducting layer layout

Conclusion

This application note shows the layout considerations, trace widths calculation and different scenario as a guideline of T1/E1 network interface with DS26528. The guideline is applicable for other Dallas Semiconductor T1/E1 products.

If you have further questions about our T1/E1 products, please contact the Telecommunication Applications support team via email telecom.support@dalsemi.com or call 972-371-6555.

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